FORMATION OF HERMETICALLY SEALED DIELECTRICALLY INSULATING ISOLATION TRENCHES

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The invention relates to a method and an assembly for forming structures that are dielectrically insulated from each other by means of filled hermetically sealed isolation trenches for the formation of mechanical-electrical sensor structures, which require for their functioning a hermetically sealed cavity, in which are located the moveable sensor elements. The conventional isolation trenches for the dielectric insulation of different electronic circuit portions do not automatically meet the requirements for the formation of microelectro-mechanical systems (MEMS), in which the formation of the cavities for the mechanically moveable sensor elements is also required across circuitries or circuit portion isolated from each other by trenches.

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Filled trench structures are used, for instance, for the dielectric insulation of high voltage elements, cf. **DE-A 198 28 669,** or for the dielectric and capacitance-reduced insulation in integrated HF elements and for the formation of insulated portions for electromechanic structures, cf. **DE-C 100 29 012.** Filled trench structures are preferably used for SOI wafers, as well as for single-crystalline semiconductor wafers for the dielectric peripheral insulation of source/drain portions in CMOS circuits, cf. **DE-A 197 06 789.**

The electrical, mechanical and thermal requirements for such trench structures and the filling thereof are different depending on the technology and the preceding technology steps (for instance, integration in a CMOS technology). For this reason, also different materials and methods are used for the filling of such electrically insulating trench structures. The materials used are preferably silicon dioxide, silicon nitride, polysilicon or organic materials, such as polyamide. Generally, priority is given to a void free or void reduced filling so as to avoid any gas enclosures. The methodological conditions therefore may, however, match those required for highly integrated circuit technology and require high efforts in case the conditions have to be correspondingly adapted.

In most situations, the shape of the trenches is selected so as to exhibit vertical walls or so as to exhibit a v-shaped tapered portion in order to facilitate a void free filing, cf. **JP-A 2002 100 672,** "Forming Method of Isolation Trench." The advances in this field also refer to mechanical electrical structures as a part of the complex semiconductor manufacturing process (for instance, CMOS technology) and, thus, require the realization of hermetically sealed cavities for the functioning of these mechanically moveable structures, cf. **DE-A 100 17 976.** During the filling of the trenches, channel-shaped cavities may readily be formed in the interior of the trench caused by a rapid growing together of the fill material at the upper side of the trench, starting from the upper trench edges. The cavities or voids may tunnel through the boundary of the sensor cavity that should hermetically be sealed, thereby resulting in a failure of the device owing to damage of the actual sensor element.

For sophisticated requirements with respect to the trench geometry, when vertical sidewalls or v-shaped cross sections may not be realized and under-cut edges are admissible, new approaches have to be found.

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It is the object of the invention to overcome the deficiencies described above that occur during the filling of isolation trenches having a standard cross sectional shape, which may be associated with void or cavity channels that laterally extend and that are produced during the filling process, in order to insure the hermetical sealing of the cavity for the mechanical electrical structures in combination with the hermetically sealed wafer bonding. Moreover, a simple and cost efficient method is to be provided, which insures a hermetical sealing of possible void channels, which may form in the lateral direction during the filling of isolation trenches. Wafers processed in such a manner should be able to be subjected to a further standard CMOS processing.

The object is solved in accordance with the present invention in that, at at least one defined position in the trench in a short portion (section), the trench is broadened or enlarged with a small amount (sealing point or position), and in that a deposition technique (low pressure deposition) is used for the deposition of the film material for sealing the trench, wherein the method is performed nearly at vacuum (claim 1 or 5). The result of this is a trench geometry having at least two

narrow sections and a broader intermediate section connecting these two narrow sections (claim 13).

The sealing positions or points may be replicated several times, depending on the requirements.

The principle of the sealing is based on a three-dimensional filling process in the vicinity of the respective sealing point. The locations of the broadened trench remain unfilled (open) for a prolonged time period during the deposition of the layer for filling the trench compared to the immediately neighboring trench portions having the standard width.

When the standard trench is closing during the fill process and parasitic voids have already formed therein, in general there is no longer the possibility to supply further material for the filling of these remaining voids or cavities. According to the present invention, however, also a lateral deposition in the lateral direction of the trench will occur resulting from the broadened trench area, which is still open at this time. This lateral deposition results in a filling of the remaining voids from the front side (three dimensional filling) and clogs the void in the normally broad channel area of the longitudinal side before the somewhat broader channel position also slowly closes in the upward direction, where typically a somewhat larger remaining void is formed, which does not result in a negative effect, since a hermetic seal is obtained on both sides and in the upward direction.

As a result of this hermetic sealing, any post-process gas exchange and thus any negative characteristic of the gas passage in laterally formed voids or cavities and filled trenches may be avoided.

The deposition method performed approximately at vacuum (claim 10) results in an approximately isotropic filling of the broadened trench sections and insures within the parasitic remaining voids or cavities that a (approximately "good") vacuum remains.

Since now (substantially) no gas is located within the hermetically sealed remaining voids, even high temperature processes may subsequently be applied without having to consider the cracking of such remaining voids.

With respect to the shape of the trench and the slope of the sidewalls, this method may not need to meet particular requirements.

The solution of the present invention gains particular importance when remaining voids may not be avoided without additional effort during the filling process.

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The invention will now be explained and completed by means of exemplary embodiments, wherein it is to be appreciated that in the following description preferred embodiments of the present invention will be described.

Figure 1 is a schematic illustration in plan view of a slight channel broadening 2 introduced into a trench (channel).

Figure 2, figure 2a, figure 2b represent a schematic illustration and two sections A-A and B-B of a slight broadening introduced into a trench, wherein the trench regions having the normal width b1 are already closed towards the trench top. A layer deposition only occurs in the slightly broadened channel region 2.

Figure 3, figure 3c depict the trench filling 9 and the trench broadening b2 (channel broadening) and the closing of parasitic remaining voids.

Figure 4, figure 4d, figure 4e, figure 4f illustrate the result of the trench filling 9 with hermetical sealing of the parasitic remaining voids in the trench region by means of various trench cross sections (figure 4d, e, f) at different positions of the total trench 1, 2, 1 according to figure 4.

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Figure 1 depicts the trench broadening 2 as a channel broadening b2, which with both sides (the front ends) is located adjacent to the trench region 1 (channel) having the normal width b1. The transition portion 3 between both trench regions should be of conical form. Shown in **figure 2** and the sections of the **figures 2b, 2a** is in a schematic diagram a layer deposition on both sidewalls 4. The deposition (cf. black arrows figure 2b) occurs identically on the sidewalls 4 within the area of the slight trench broadening 2, figure 2b, after the trench is already closed in the upward direction within the region 1, thereby resulting in a small void-channel 5, figure 2a. The trenches (the channel) are located within the silicon environment 10.

The trench filling 9 is a fill material, which is deposited. The fill material insures that the trench sections 1 of normal width in figure 1 (at the left side and the right side of the conical enlargement of the trench width b1 towards the slightly broadened trench width b2 of the section 2) are closed. During the filling within the area of the trenches of normal width the upper trench areas are closed earlier compared to the trench section 2 having the enlarged width b2. In the upper trench area fill material is present at this time, wherein a void or cavity (void channel 5) may form in the longitudinal direction of the trench, that is, the sections 1 of figure 1 or figure 2. By means of a low pressure material deposition in the broadened trench area (the longitudinal section 2), the void channels in the longitudinal directions are hermetically sealed. This material deposition is a low pressure material deposition, in which a pressure approximately at vacuum is used. Thereby, a layer deposition method is used, which results in a substantially isotropic filling of the broadened trench section. Parasitic voids remaining at this position will exhibit substantially no pressure and may rather exhibit an approximately good vacuum due to the low pressure deposition technique.

The sealing is performed on the basis of a filling process occurring in every direction (three-dimensional filling) of the trench along its total longitudinal direction, to which belong the narrow sections 1, the conically tapered sections 3 and the slightly broadened trench section 2 having the width b2. There may be a plurality of these sections arranged to form a corresponding sequence of which in figure 1 merely one broadening is shown that has adjacent to it conical sections 3 and narrower channel sections 1.

The at least one position 2, - for a plurality of sections 2 the plurality of slightly broadened trench sections - remains open for a prolonged time period during the

layer deposition for the filling compared to the sections 1 having the normal width b1. From the broadened trench region 2, which is still open at the time of closing the narrower sections 1 (open in the upward direction) there may now occur a lateral deposition in the lateral direction of the trench progression. This lateral deposition results in a filling of the remaining voids from the front side as a three-dimensional filling and also clogs the (parasitic) void in the channel region 1 having the normal width starting from the longitudinal side. Only at a later stage the broader channel section also slowly closes in the upward direction, thereby forming a somewhat larger void, which is indicated in figure 2b (the inner open area) and which is described in more detail in the subsequent figures. This section is not critical, since a hermetic sealing is formed at both sides and in the upward direction.

A subsequent gas exchange is avoided. There remains substantially no gas under pressure within the voids so that subsequent processes may be performed with an arbitrary temperature without a risk of cracking of closed channels owing to overpressure forming in the voids 5 or within the larger voids 8 that will be described with reference to figure 4f.

Contrary to well known techniques trying to avoid voids, the method explained with reference to figure 2, which is discussed in even more detail on the basis of the subsequent figures, may tolerate such voids, but, nevertheless, avoids any difficulties that may result during the further processing. The isolation trenches or, in short, "trenches," are filled by means of a deposition technique and are hermetically sealed. They are used for the dielectric insulation on the wafer.

Figures 3 and 3c schematically show a slight trench broadening 2 within a trench progression 1, cf. figure 3, wherein the trench regions 1 having the normal width b1 are already closed in the upward direction. In this stage, merely the sidewalls 4 within the trench broadening 2 are coated and also the lateral filling of the parasitic remaining voids at the location of the lateral filling 6 occurs in accordance with the present invention, cf. figure 3c.

Selecting the parameters of the deposition and of the trench arrangement is performed such that possibly remaining lateral voids are completely sealed prior to the closing, in the upward direction, of the trench section having the slight broadening so that a further filling may not be allowed to occur.

The layer deposition in figures 3 and 3c occurs only in the broadened channel section 2, that is, in its region, wherein the lateral filling of the residual remaining voids is emphasized.

Figures 4, as well as the sections of **figures 4d, 4e, 4f,** schematically illustrate the results of the completed trench filling. Figures 4d to 4f represent three sectional diagrams along the planes E-E, F-F and G-G in figure 4.

Figure 4d section D illustrates the smaller remaining void 5 in the normal trench region 1.

Figure 4e section E illustrates the hermetical seal 7 in the area of the conical intermediate or transition portion 3.

Figure 4f section F illustrates the somewhat larger remaining void 8 in the area of the slight trench broadening 2, which is also covered by fill material 9.

Figure 4 represents a plan view of the trench region to be filled in the sections 1, 2 and again 1. The corresponding components of figure 1 may also be applied here without changes.

The slight trench broadening according to the width b2 (i.e., b2-b1) and the conical transition portion 3 having walls that are oblique with respect to the middle plane are evident from the figures. There are two transition portions 3 per each slightly broadened trench section 2 for the total trench 1, 2, 1. It is also denoted as a channel. In the sectional illustration, the section D-D is provided in the area of the narrower trench section 1. A smaller remaining void 5 is indicated, which is on its upper side already closed by fill material 9. A further section plane E-E, which is located more downwardly in figure 4, illustrates a hermetical seal at the sealing position 7, which is also referred to as "sealing point."

A sealed void or inner channel 5 may no longer be seen. The hermetical sealing 7 is performed at a position of the lateral filling 6. The hermetical sealing 7 is located in the area of the conical section 3.

The lateral filling 6 is located closer to the narrower section 1, whereas closer to the broadened section 2 or within the broadened section 2 is located a somewhat

enlarged remaining void 8 that is also closed by fill material 9, the upper portion of which, however, has been closed during a later stage of the method compared to the closing process 9 of figure 4d.

The silicon environment of the wafer is denoted as 10 similarly as in all other examples.

The broadened trench positions 2 in the form of "sealing positions" of the channel in the vicinity of the bond surfaces of two semiconductor wafers are positioned more densely during the bonding of these wafers than along the other portions of the isolation trenches (not shown in the figures).

The application of the method also results in the illustrated trench structures according to the previously described method but in the form of a device on or with a wafer comprising isolation trenches, which are hermetically sealed and are used for the dielectric insulation. The process of filling of the trenches was accomplished by a deposition technique as is described.

Table of Reference Signs

Figure 1

1: trench region to be filled
2: light trench broadening
3: conical transition portion

Figures 2, 2a, 2b

1: trench region to be filled
2: slight trench broadening (trench that is slightly broadened)
4: sidewalls of the slight trench broadening
5: all remaining voids in the area of the normal trench region
9: material for filling the trench
10: silicon environment
--> arrows between the walls 4: direction of the layer deposition

figures 3, 3c

1: trench region to be filled
2: slight trench broadening
3: conical transition portion
4: sidewalls of the slight trench broadening
5: small remaining voids in the area of the trench region 1 having the normal width
6: position of the lateral filling
9: material for the filling of the trench
10: silicon environment
--> arrows between the walls 4: direction of the layer deposition

figures 4, 4d, e, f

1: trench region to be filled
2: slight trench broadening
3: conical transition portion
5: small remaining void in the area of the normal trench region
6: position of the lateral filling
7: position of the hermetic sealing in the area of the conical transition zone
8: somewhat larger remaining void in the area of the slight trench broadening
9: material for the filling of the trench
10: silicon environment